ABSTRACT

A method is provided for manufacturing a MirrorBit® Flash memory with high conductivity bitlines and shallow trench isolation integration. A hard mask is formed over a substrate and used to form a core trench and a shallow trench isolation (STI) trench. The trenches are filled with an insulating material in an STI fill process. A core mask is formed over the STI trenches and exposing the core trenches. The insulating material is removed from the core trenches and the core and hard mask are removed. A doped bitline material is deposited on the surface of the semiconductor, which fills the core trench. The surface of the semiconductor is planarized, inlaying insulating material and doped bitline material in the trenches. A thermal anneal causes the dopant diffusion from the doped bitline material into the substrate to form the high conductivity bitlines.